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Testing Considerations for High-Density Co-Packaged Optical Devices

WHITE PAPER

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Introduction

The networking devices used in datacenters, machine learning, and artificial intelligence (AI) applications must communicate large amounts of data rapidly. As a result, bandwidth requirements for network switches have grown by more than 8,000 percent in just over a decade. As shown in Figure 1, switch speed requirements have grown from 320Gb/s in 2010 to 25.6Tb/s in 2022, and are well on the way to needing to exceed 51.2 Tb/s.

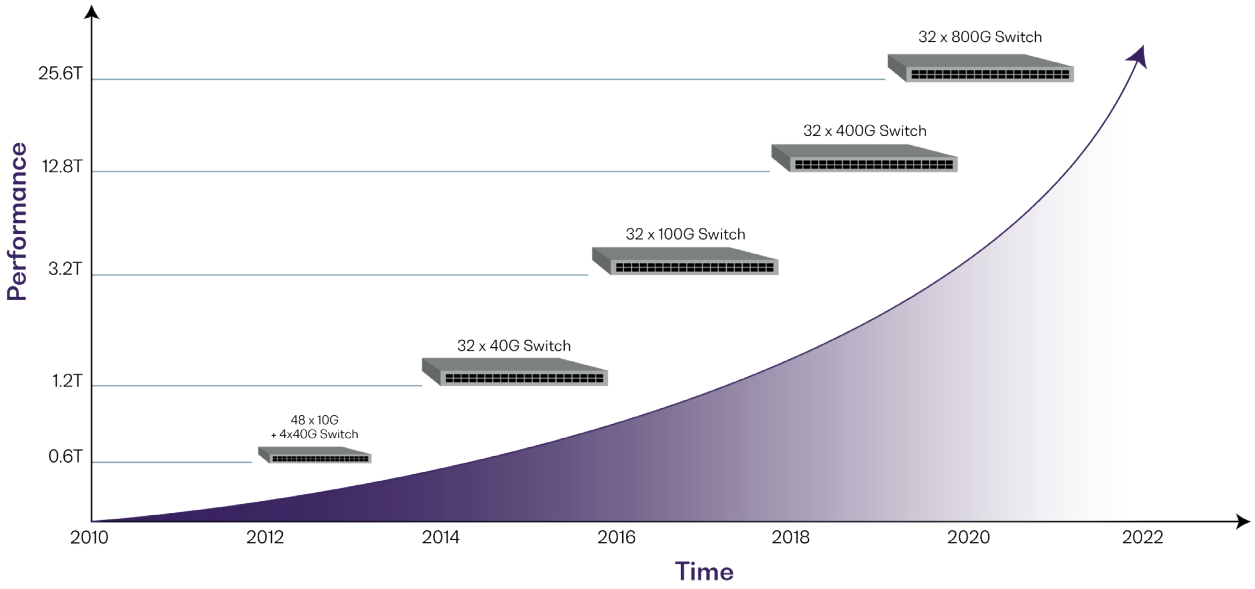


Figure 1:

The rapid increase in the need for optical devices to power data-intensive applications is driving the demand for higher performance, higher bandwidth network switches.

Achieving the high-channel counts required to reach bandwidths of more than 25.6Tb/s is very challenging if the current approach of using pluggable modules that insert into the faceplate of the rack mount switch is not disrupted. Using pluggable models at these high bandwidths leads to large energy losses when running the electrical signals from just behind the front panel to the switch ASICs and requires power-hungry signal processing to overcome channel impairments. Together, these issues directly lead to the high-power consumption and the associated high operating expenses to cool the pluggable optical transceivers and switches.

To address these challenges, and eliminate data transmission bottlenecks, optical engineers are developing more efficient means to bring the optical channels closer to the electrical devices. Many large technology companies and optical standards organizations support the idea of removing the transceivers from the front panel to create a single packaged device that brings the data right to the electrical switching fabric. Known as a co-packaged optical device, this technology can increase bandwidth without greatly increasing energy consumption or transceiver footprint as the optics and electronics sit directly next to each other in a single packaged assembly. This design minimizes transmission losses and decreases signal processing demands to offer the lowest possible power per bit for data transmission.

As with any new technology, engineers not only need to work through the complexities of developing the actual devices, but they also need to have the instrumentation available to quickly test the functionality of these channel-dense devices.

This white paper provides an overview of the work underway to ensure the interoperability of co-packaged optical devices for a variety of high-bandwidth applications and discusses how to address the testing challenges coming with this new technology.

Ensuring Interoperability & Standardization of Co-Packaged Optical Devices

Currently, the Optical Internetworking Forum (OIF) and Consortium for On-Board Optics (COBO) are iterating on framework and specification documentation for co-packaged optical device development. At a high-level, the OIF framework focuses on addressing the application spaces and relevant technology considerations for co-packaging of optical and electrical communication interfaces. This framework also provides a number of technical considerations for designing co-packaged optical devices that will meet the goals of reducing power consumption as bandwidth requirements increase.

The OIF also has a related secondary initiative in place that covers the use of external laser sources, such as external laser small form pluggables (ELSFP), to extend the reliability and longevity of co-packaged optical devices. With the COBO specification, the main goal is to ensure a consistent platform for end users of this technology by providing common specifications for system manufacturers and integrators, component manufacturers, and suppliers of 8-lane and 16-lane on-board optics.

Key Application Areas for Co-Packaged Optical Devices

The OIF identified the following three key applications that can greatly benefit from the low-power and high-bandwidth co-packaged optical devices will offer:

- Data center Ethernet network interface controllers (NICs), switches connecting servers, and storage devices
- AI GPU interfaces used for training and machine learning
- Disaggregation

While each application has unique requirements and operates in a different environment, each use case has the same basic architectural needs that includes two communications endpoints with high bandwidth requirements. Figure 2 shows how a co-packaged optical device can be configured to address the needs of each of these unique applications.

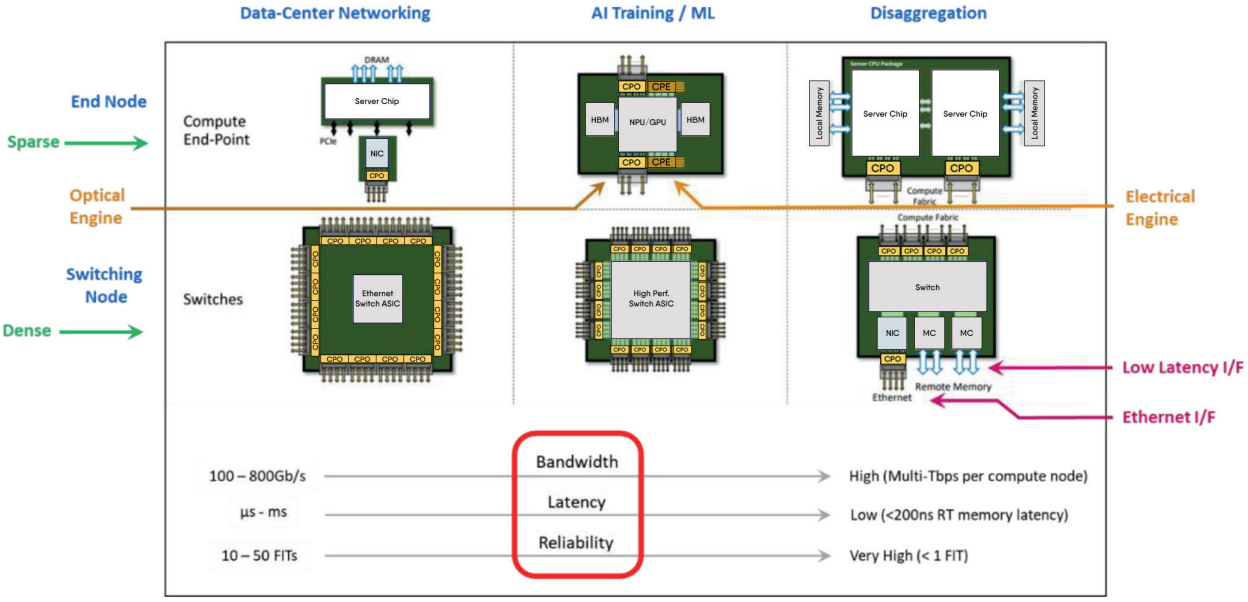


Figure 2:

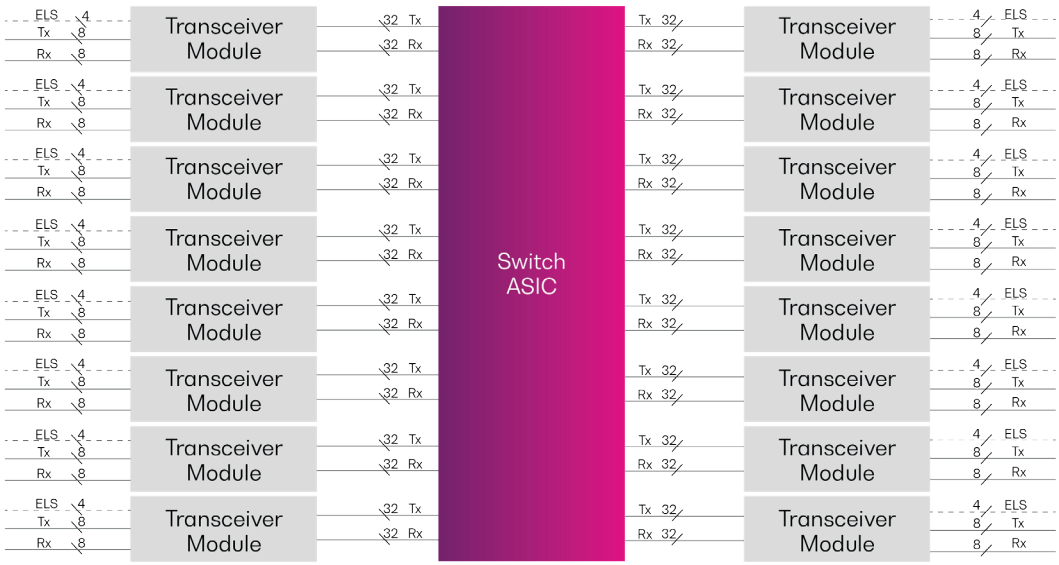
Potential architectures for co-packaged optical devices that can meet the bandwidth, latency, and reliability needs of different applications. Source: OIF Forum.

The Building Block of a Co-Packaged Optical Device: A 3.2Tb/s Optical Module

In 2021, the OIF started a project to provide a framework for the development of a 3.2Tb/s module (and eventually a 6.4Tb/s module) that could serve as the building block for the 51.2 Tb/s switch. Ultimately, the architecture proposed by the OIF and COBO is based on the 51.2 Tb/s switch including 16 of the 3.2Tb/s modules arranged near the ASIC as shown in Figure 3.

Figure 3:

A system block diagram for a 400GBase-FR4 3.2Tb/s module.



Currently, many OIF members working on the 3.2Tb/s Co-Packaged Optical Module Implementation Project are developing 400GBASE-FR4 and 400GBASE-DR4 options that have backwards compatibility to 200G interfaces. While all the requirements for these devices are detailed in this product requirements document (PRD), some of the key guidelines of this project include the following:

- A module should include a digital signal processor (DSP), a modulator driver, transimpedance amplifier (TIA) chips, and an optical Tx/Rx combination based on silicon photonics regardless of operating mode
- The transceiver's electrical interface shall be based on 32 × 106G electrical lanes in compliance with CEI-112G-XSR and the electrical interface rates shall drop to 32×53G PAM4 when in 200BASE-FR4 operation
- To keep the module size as compact as possible, there shall not be an internal power supply unit

Since the optical and electrical interfaces are key components of these modules, let's further explore the OIF framework guidance provided for these components.

Optical Interfaces

Under the OIF framework, co-packaged optical modules shall be based on existing optical interface standards including VR4, SR4, DR4, and FR4. As shown in Table 1, the 400GBase modules have different reaches, wavelengths, and channel counts. Different test parameters will be required depending on the standard selected.

	Reach	Symbol Rate	Modulation	Wavelength	Wavelengths per Fiber Pair	Number of Fiber Pairs (Tx/RX)
400GBase-VR4	500 m	53.125 Gbaud	PAM4	850 nm	1	4
400GBase-SR4	100 m	53.125 Gbaud	PAM4	850 nm	1	4
400GBase-DR4	500 m	53.125 Gbaud	PAM4	1311 nm	1	4
400GBase-FR4	2 km	53.125 Gbaud	PAM4	1271, 1291, 1311 and 1331 nm	4	1

Table 1:

An overview of the specifications for optical interfaces designed using different common standards.

Since the standards used for these optical interfaces are the same as those used for today's pluggable modules, interoperability between co-packaged modules and pluggable devices is preserved. Therefore, a datacenter could have a fiber breakout cable with a pluggable module at the end to allow for the best mix of pluggable and co-packaged modules to meet their needs.

Electrical Interfaces

While co-packaged applications may use a variety of electrical interface standards such as XSR, LR, PCIe, or AIB, the OIF framework mainly focuses on using XSR. An example of a module using XSR is shown in Table 2 over the next page.

Table 2:

The specifications for a module using an electrical interface based on the XSR standard.

Electrical Channels	Reach	Symbol Rate	Modulation	Number of Channel Pairs
CEI-112G-XSR-PAM4	50 mm	53.125 Gbaud	PAM4	4

Additionally, the OIF framework suggests that the following four electrical interface options can be used in a co-packaged optical module:

- Retimed – Uses the CEI-112G-XSR-PAM4 implementation detailed in Table 2 and is designed for low error rate communications between the ASIC and optical engine over ~50mm of first level packaging substrate.
- Linear Amplified – The CDR/DSP function in the engine is eliminated to reduce power consumption and the Tx and Rx functions in the ASIC have more amplification and peaking so that the SerDes can compensate for the entire link.
- Half Retimed – Half of the engine and ASIC communication is re-timed, and the other half uses a linear-amplified approach.
- Direct Drive – This is a simplified interface that provides only the functions necessary to support a linear optical communications channel.

Review the OIF framework and the optical module PRD for more details on the proposed electrical and optical interface specifications.

Laser Placement for Co-Packaged Optical Modules

As the community works to develop a 3.2Tb/s module, there is a debate on where the laser should be located – internally or externally. Since the laser is the module component most likely to age and generates a large amount of heat, reliability and system cooling are concerns for using an internal laser. To address reliability issues, one option proposed is to include a back-up laser in the module for redundancy. The concern with this approach is that it will increase the module's footprint, which is not ideal for many applications.

Research on external placement of the laser is also in the works by OIF community members through the ELSFP Module Project previously mentioned. External laser placement makes the assembly smaller, eliminates thermal challenges associated with using an internal laser, and generally improves module reliability. However, the biggest drawback of using an external laser source is that insertion loss to couple the laser into the module will increase. To compensate for this, the laser's output power needs to be up to 22dBm per wavelength, which will increase energy consumption.

Addressing Three Big Testing Challenges for Co-Packaged Optical Devices

The development of new technology invariably creates new testing challenges for optical engineers. To ensure faster implementation and deployment of new devices, test requirements from qualification, to high-volume manufacturing should be considered in parallel with device development. While the first half of this white paper focused on some of the key elements of co-packaged optical device development, the focus will now shift to examining three of the main testing challenges for producing this technology.

Challenge 1: Rapidly Performing Assembly Testing

As mentioned, a co-packaged optical device consists of a collection of individual transceiver modules – 16 units of 3.2Tb/s for a 51.2Tb/s co-packaged device for example. Each transceiver module is assembled from dies that originate from one or multiple wafers. To reduce the chance of an issue occurring late in the assembly process, lessons learned from decades of high-volume semiconductor manufacturing can be applied to the optical testing needed for co-packaged optical devices.

Let's examine the following test phases needed with this testing approach:

- Wafer testing
- Module testing
- Co-packaged assembly testing

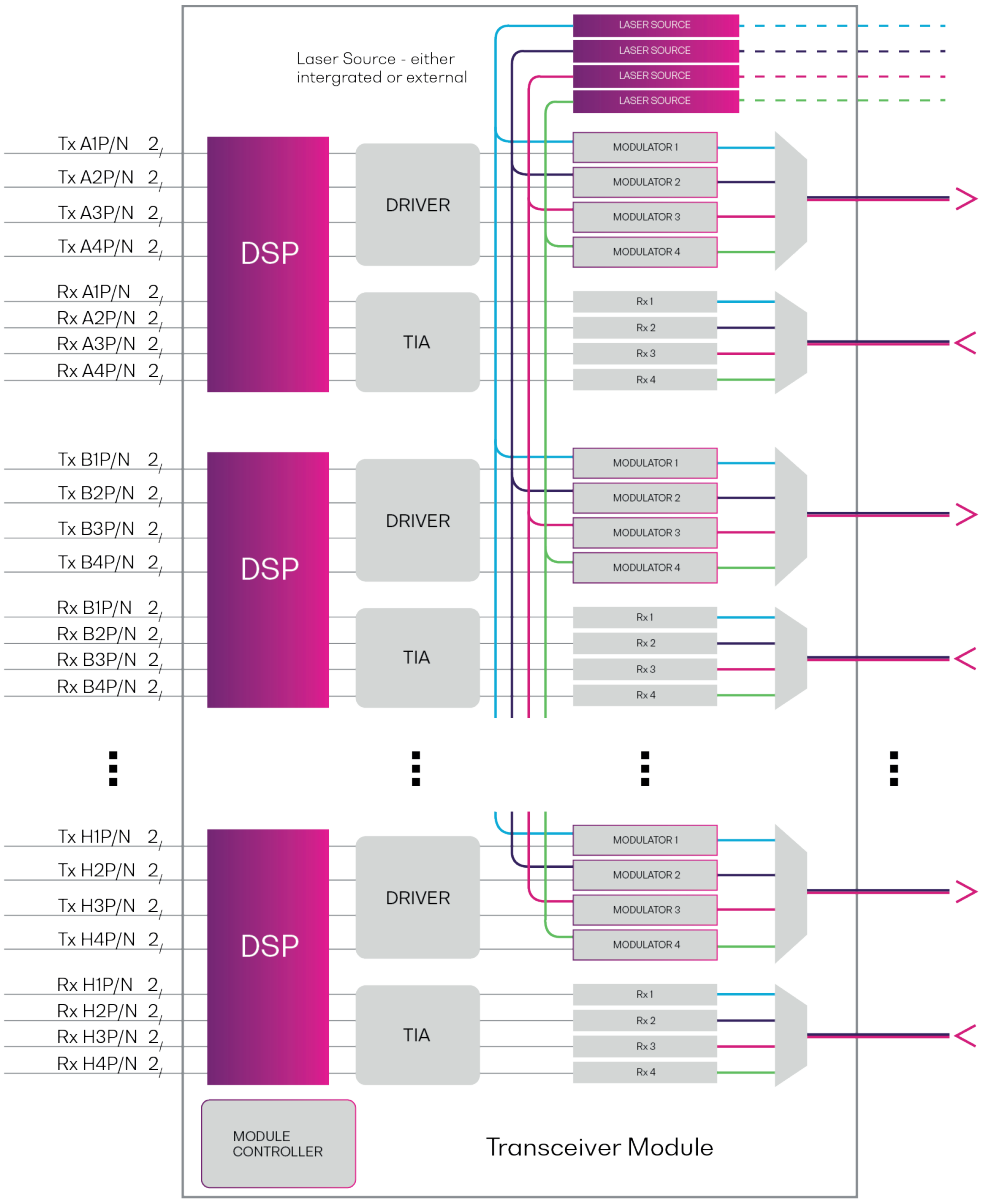
Wafer Testing

Wafer testing is a critical first testing step as it is the least costly place to catch a failure. Once resources are invested in dicing up the wafer and creating a module, manufacturers need to be sure that the components making up the module are up to spec. To be confident there are not any critical performance issues that will impact yield, high-throughput wafer-level testing is needed early in the fabrication process, yet this type of testing for silicon photonics presents a number of challenges.

While there are some parallels with semiconductor wafer testing, testing with photons is very different from testing with electrons. For example, electrical testing can be done by creating a conductor connection with a probe card, but for optical testing, tight alignment is needed to couple light into and/or out of the photonic components. To achieve the alignment necessary for injecting and capturing light for these tests, optical probes need to be robotically manipulated around the wafer. Furthermore, to perform these tests at high volumes, rapid active alignment is necessary. Quantifi Photonics' logarithmic analog power meters are a good example of equipment designed specifically for wafer testing, allowing very high speed fiber alignment.

Figure 4:

An example of a potential module configuration. Source: OIF Forum.



Module Testing

Modules are assembled by packaging the appropriate number of dies that passed wafer testing and connecting the dies with the other elements necessary for the module such as the lasers, amplifiers, modulators, and basic components needed for signal processing. Module testing is the first opportunity to test the full performance of a unit. This can include a variety of tests such as those that look at the modulated optical signals, lasers, thermal cycling and calibration of the module and it can also include loop back and bit error rate testing (BERT) for the full module, over the required reach budget.

Testing at this level can be challenging for a few reasons. First, modules can use a variety of different optical and electrical standards as discussed in the first part of this paper, which means there is different performance criteria that need to be understood and tested for each module configuration. Right up-front, volume projections will dictate if the test station will be tailored for a single flavor of module like SR4 multimode 850nm, for example, or if it should be configurable to handle a number of different flavors like SR4 and FR4, which use different fiber types and wavelengths.

Additionally, in a 3.2Tb/s module for example, there are 8 fibers that each have 8 wavelengths, which means there are 64 channels to test. Without test equipment that supports parallel testing, a number of switching matrices are needed to switch between the different fibers in the multifiber arrays or to switch out the different wavelengths to an oscilloscope for TDEQ measurements. This switching approach is more time consuming and likely to also increase testing cost per unit compared to parallel testing as it takes time to change out tests.

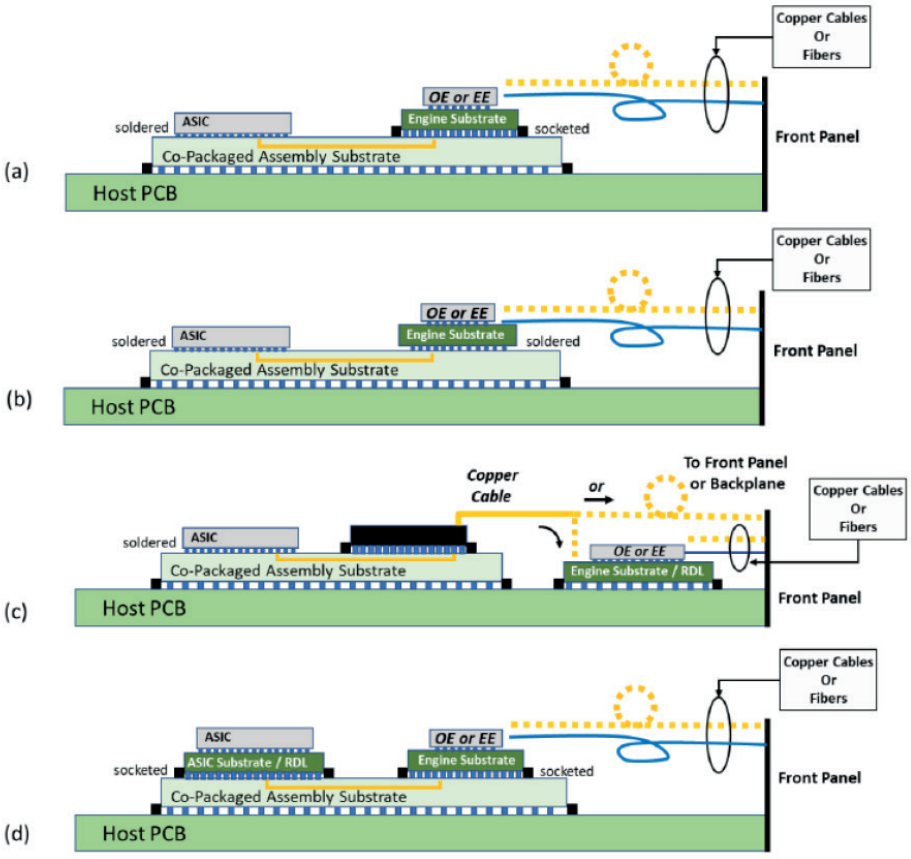
Instead, high-density test equipment that supports rapid parallel testing, such as our BERT, presents a much better way to test the multiple fibers and wavelengths in these modules. With this type of high-density, high-channel test equipment, users have the flexibility to perform testing in a variety of ways. For example, eight fibers can be tested at one time, and wavelengths for parallel testing can be demultiplexed.

Co-Packaged Assembly Testing

This final level of testing involves testing the fully tested modules once integrated with the ASIC and other necessary components. A few possible assembly options for co-packaged assemblies are shown in Figure 5 below.

Figure 5:

Illustrations of four different assembly options for co-packaged optical devices. Source: OIF Forum.



At this point, functional testing is needed to ensure all parts of the assembly were integrated correctly without introducing manufacturing defects such as the misalignment of modules, pinching of fibers, or damage to ports. However, with assembly testing, test challenges are multiplied again. For example, if an assembly incorporates eight modules each with 8 fibers and 8 wavelengths per fiber, there are now a total of 512 channels to test. So, if a single-channel module test were to take one minute to perform, it is not practical to test all 512 channels using a single-channel test method.

Parallel testing is therefore a critical success factor on the production line and commercial test and measurement vendors are racing to keep up. Testing equipment such as our high-density power meter that can scale to perform parallel testing of up to 288 channels are key to taking the rapid measurements necessary for testing the performance and power of the optical signals in these assemblies.

Challenge 2: Parallel Assembly Needs Parallel Testing

Traditionally, optical devices are tested once all components are assembled. While this approach allows for rapid device assembly, it can lead to a need to increase test coverage and contribute to poor yield. Instead, it is better to test during device assembly as this method provides instant feedback to ensure successful assembly.

Let's look at a simple example comparing these two test approaches. If a device is assembled using an MPO-24 fiber ribbon with a traditional assemble-then-test approach, testing during assembly will likely only be performed on one fiber in the ribbon to ensure the assembly method worked. The assumption is that this same assembly method will then be successful for the other fibers in the ribbon. However, since optimal alignment of just that one fiber was checked, performance of the other 23 channels may be sacrificed to achieve the best performance on just one fiber. Instead, with the right equipment for performing parallel assembly and testing, it is possible to optimize the assembly for the full ribbon. To do this, test instruments that offer multi-channel testing such as lasers, power meters, attenuators, and switches are necessary.

Challenge 3: Eliminating Captive Instruments

Ensuring optimal utilization of test instruments when performing parallel test can be tricky. It is easy to have test setups with captive instruments, or instruments that are underutilized or used inefficiently in the test station. This can happen in parallel testing operations when an instrument such as an optical spectrum analyzer (OSA) is used to perform a test for 80 milliseconds, yet tests with other instruments to perform PAM4 TDEQ can take tens of seconds. The instrument that is only needed for 80 milliseconds is likely sitting idle most of the time.

To maximize instrument utilization and reduce the total cost of a test system, it is best to optimize test processes to use both serial and parallel testing together. This testing approach requires versatile optical switches to breakout the parallel ports or move the parallel ports at the same time to provide the flexibility to pull out certain channels or move channels as needed.

Overcoming Today's Testing Challenges and Scaling for the Future

To keep up with the rapidly increasing bandwidth demands of many applications without greatly increasing energy usage and the footprint of networking applications, co-packaged optical devices are a promising solution. While many organizations are collaborating to develop the necessary technology for these modules, there are current, and future testing challenges for these devices that must be considered and overcome.

At Quantifi Photonics, we recognize the urgency of supplying high-channel, high-density test equipment that will help make the proliferation of co-packaged optical devices a reality. We have already released several products that enable some of the required testing, and we have an extensive road map in place to help address current bottlenecks for these tests. As part of our vision, we are working to help the photonics industry achieve the full automation level that is common in electrical semiconductor test. We envision a future where high-throughput testing is not only possible, but the testing instruments used also offer a convenient and compact form factor that will help companies continue to optimize their test setups and rapidly innovate.

Test.
Measure.
Solve.™

Quantifi Photonics is transforming the world of photonics test and measurement. Our portfolio of optical and electrical test instruments is rapidly expanding to meet the needs of engineers and scientists around the globe. From enabling ground-breaking experiments to driving highly efficient production testing, you'll find us working with customers to solve complex problems with experience and innovation.

To find out more, get in touch with us today.

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